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1. **Automatic Josephson-transmission-line routing for single-flux-quantum cell-based logic cir**
Kameda, Y.; Yorozu, S.;
Applied Superconductivity, IEEE Transactions on
Volume 13, Issue 2, Part 1, June 2003 Page(s):519 - 522
Digital Object Identifier 10.1109/TASC.2003.813922
AbstractPlus | References | Full Text: PDF(552 KB) IEEE JNL
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2. **Coupling-aware Dummy Metal Insertion for Lithography**
Liang Deng; Martin D. F. Wong; Kai-Yuan Chao; Hua Xiang;
Design Automation Conference, 2007. ASP-DAC '07. Asia and South Pacific
Jan. 2007 Page(s):13 - 18
Digital Object Identifier 10.1109/ASPDAC.2007.357785
AbstractPlus | Full Text: PDF(191 KB) IEEE CNF
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3. **BEOL process integration technology for 45 nm node porous low-k/copper interconnects**
Matsunaga, N.; Nakamura, N.; Higashi, K.; Yamaguchi, H.; Watanabe, T.; Akiyama, K.; Nakao, S.; H.; Omoto, S.; Sakata, A.; Katata, T.; Kagawa, Y.; Kawashima, H.; Enomoto, Y.; Hasegawa, T.; Sh
Interconnect Technology Conference, 2005. Proceedings of the IEEE 2005 International
6-8 June 2005 Page(s):6 - 8
AbstractPlus | Full Text: PDF(203 KB) IEEE CNF
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IEEE STD	IEEE Standard

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Semiconductor device having a multilayered wiring structure with ...
The present invention is characterized in that a **dummy wiring** is provided between wirings constituting a multi-layered wiring, when an electric connection ...
www.patentstorm.us/patents/5442236-claims.html - 20k - Cached - Similar pages

Multilayered wiring substrate with dummy wirings in parallel to ...
a dummy through hole extending in said stacking direction, disposed adjacent to said **dummy wiring** on the side on which said signal wiring group is present; ...
www.patentstorm.us/patents/6630627-claims.html - 18k - Cached - Similar pages
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Semiconductor device with **dummy wiring** layers - Patent 6504254
A semiconductor device 100 has wiring layers 20a and 20b and a plurality **dummy wiring** sections 30 provided at the same level where the wiring layers 20a and ...
www.freepatentsonline.com/6504254.html - 40k - Cached - Similar pages

Method of designing **dummy wiring** - Patent 6253362
Wiring of a non-uniform density is laid out on a chip. Then, the chip is virtually divided into a plurality of sub chips. The wiring density of each sub ...
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[PDF] Mechanism of Moisture Uptake Induced Via Failure and its Impact on ...
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density close to via and **dummy wiring** pattern area size. strongly affect via resistance ...
upper metal connected the vias to **dummy wiring** on the via ...
ieeexplore.ieee.org/iel5/10701/33791/01609301.pdf - Similar pages

[PDF] BEOL Process Integration Technology for Node Porous Low-WCopper ...
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Dummy wiring pattern was also adopted to remove. moisture absorbed in porous low-k films. ... **dummy wiring** pattern for enhancing outgas from the ...
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Computex Taipei 2006
ADP-2042DIN(R), DIN rail mounted wiring board matched MPC-2042/3042,General output: 8 relays. 6. JD50095, DIN rail mounted **dummy wiring** board (for JF2) ...
www.computex.biz/computex2006/productnews_skeleton.asp?index=26977 - 24k - Cached - Similar pages

esp@cenet document view
CONSTITUTION: The starting film of scanning line is patterned, **dummy wiring** 301 of 1st layer in the shape of, rectangular pole not to be connected ...
v3.espacenet.com/textdoc?DB=EPODOC&IDX=KR100383163B&F=0 - 36k - Cached - Similar pages

Toshiba : Press Releases 7 December, 2005
In seeking improved low-k film technology, Toshiba and Sony enhanced the quality of the

low-k film by appropriately allocating **dummy wiring** to improve ...
www.toshiba.co.jp/about/press/2005_12/pr0701.htm - 10k - Cached - Similar pages

EP949572 Nippon european software patent - Arranging/wiring method ...
[0044] Further in this case, the arranging the first **dummy wiring** line includes ... In this step, since the above-explained virtual **dummy wiring** line 3 is ...
gauss.ffii.org/PatentView/EP949572 - 96k - Cached - Similar pages

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"dummy wiring" Search

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Semiconductor device - Patent 20040222531
A semiconductor device according to claim 10, wherein a **dummy wiring** connected to ... and a dummy via buried in a **dummy via hole** formed in the interlayer ...
www.freepatentsonline.com/20040222531.html - 41k - Cached - Similar pages

Semiconductor device - Patent 6989583
A semiconductor device according to claim 9, wherein the **dummy wiring** layer connected to ... a dummy via buried in a **dummy via hole** formed in the interlayer ...
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Semiconductor device - US Patent 7067919
3, a **dummy wiring** 41 is provided in the non-forming region of the first wiring 36, and the **dummy via hole** 38b is formed to reach this **dummy wiring** 41. ...
www.patentstorm.us/patents/7067919-description.html - 78k - Cached - Similar pages

Semiconductor device
The dummy damaged regions 15b are formed by forming a **dummy via hole** in the ... Likewise, **dummy wiring** grooves are formed in the interlayer insulation film ...
www.patentopedia.us/latch_assembly/semiconductor.html - 51k - Supplemental Result - Cached - Similar pages

Semiconductor device patent invention
That is, each of the Cu via wirings 15 is provided as a so-called sacrificial wiring (**dummy wiring**, continuous sacrificial via layer). ...
www.freshpatents.com/Semiconductor-device-dt20070111ptan20070007618.php?type=description - 80k - Supplemental Result - Cached - Similar pages

Semiconductor chip capable of suppressing cracks in the insulating ...
The pattern of each **dummy via hole** is indicated by a rectangular frame with a cross mark. The right portion of FIG. 5A shows **dummy wiring** patterns with the ...
www.wikipatents.com/5885857.html - 146k - Cached - Similar pages

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Simulation circuit pattern evaluation method, manufacturing method ...
Incidentally, in the case of the "existence of **dummy via hole**," the states ... number of times in the respective **parameters** to make an orthogonal **state**, ...
www.freepatentsonline.com/20050075854.html - 62k - Cached - Similar pages

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Web Results 1 - 2 of 2 for "dummy wiring" "dummy via hole" state. (0.08 seconds)

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Solid-state imaging device - Patent EP1396888
The solid-state imaging device according to claim 11, wherein said dummy wiring layer and said metal wiring layer are commonly provided. ...
www.freepatentsonline.com/EP1396888.html - 57k - Cached - Similar pages

Simulation circuit pattern evaluation method, manufacturing method ...
3F, a wiring trench 3A, a dummy wiring trench group 3B, lead-out wiring trenches 3C, electrode pad trenches 3D and 3E, a via hole 3F, a dummy via hole 3G, ...
www.freepatentsonline.com/20050075854.html - 62k - Cached - Similar pages
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"dummy wiring" "dummy via hole" st Search

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8	("5442236" "6630627" "6504254" "6253362").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:39
L2	4	("5442236" "6630627" "6504254" "6253362").pn.	USPAT	OR	ON	2007/05/16 19:39
L3	1066	dummy adj wiring	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:48
L4	170	l3 and (dummy with hole)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:48
L5	47	l3 and (dummy with via with hole)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:40
L6	25	l5 and state	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:45
L7	3	l6 and parameter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:45
L8	1	l6 and (parameter same state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:45
L9	64	l4 and state	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:45
L10	5	l9 and parameter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:46

EAST Search History

L11	1	l10 and (parameter same state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:45
L12	2	l10 not l7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:46
L13	3	sacrificial adj wiring	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:48
L14	1	l13 and (hole)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 19:49
L15	0	l14 and (state or parameter)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 20:13
L16	25	l5 and (state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 20:13
L17	0	l16 and ((bar adj state) or (cross adj state))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 20:14
L18	3	l16 and ((bar with state) or (cross with state))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 20:21
L19	1	l2 and (via adj hole)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 20:21